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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,212	10/21/2003	Andrew W. Dornbusch	025.0009	8353

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/691,212	DORNBUSCH ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

(A) In Fig. 3, the reference number "340" is not disclosed in the specification of instant invention.

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 2 – 14, 16 – 20, 22 – 25 and 27 – 29 are objected to because of the following informalities:

(A) In claims 2 – 14, 16 – 20, 22 – 25 and 27 – 29, needs comma after number. (i.e., --claim 2, wherein--).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 – 3, 5 – 7 and 21 – 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Hikita et al. (U. S. Pat. No. 6,396,154).

Regarding claim 1, Hikita et al. discloses in e.g., Fig. 1 an integrated circuit (the semiconductor device in Fig. 1; column 3, lines 49 – 53) comprising:

- a semiconductor substrate (the substrate of the chip 2; column 6, lines 23 – 31) having a first pair of bonding pads (P23 and P24; column 4, lines 10 and 11) conducting a differential output signal thereon (column 4, lines 4 – 20) and adapted to be coupled to an input of a first external filter (222; see e.g., Fig. 1 and column 4, lines 10 – 13), and a second pair of bonding pads (P21 and P22) conducting a differential input

signal thereon and adapted to be coupled to an output of said first external filter (221; see e.g., Fig. 1 and column 4, lines 10 – 13); and

- an integrated circuit package (1 and 40; see Fig. 2 and column 3, line 54) encapsulating said semiconductor substrate (the substrate of the chip 2) and having first (P13 and P14) and second (P11 and P12) terminal pairs corresponding and coupled to said first and second pairs of bonding pads, respectively (see e.g., Fig. 1),
- wherein said first and second terminal pairs (P11 – P14) are separated by a first predetermined distance (the distance between the elements P11 – P14; see e.g., Fig. 1) sufficient to maintain an input-to-output isolation therebetween of at least a first predetermined amount (the amount of the gap between the elements 221 and 222).

Furthermore, it has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. In re Hutchison, 69 USPQ 138.

Regarding claim 2, Hikita et al. discloses in e.g., Fig. 1 said first predetermined amount (the amount of the gap between the elements 221 and 222) corresponding to an attenuation in a stopband of said first external filter (22; see e.g., Fig. 1).

Regarding claim 3, Hikita et al. discloses in e.g., Fig. 1 said first (P13 and P14) and second (P11 and P12) terminal pairs being located along a first side of said integrated circuit package (1 and 40) and separated by a first plurality of intervening terminals (the pads 12 that are located between the line of P11 – P12 and the other line of P13 – P14; see e.g., Fig. 1).

Regarding claim 5, the limitation "said first plurality of intervening terminals comprises at least one power supply terminal" is an intended use language that does not structurally or

patentably distinguish the claimed invention from the structure as disclosed by Hikita et al. Furthermore, since any one of the first plurality of intervening terminals is capable of performing as a power supply terminal, Hikita et al. fully meets this limitation.

Regarding claim 6, Hikita et al. discloses in e.g., Fig. 1 first (P13) and second (P14) terminals of said first terminal pair (P13 and P14) being "adjacent" to one another (see e.g., Fig. 1), and first (P11) and second (P12) terminals of said second terminal pair (P11 and P12) are "adjacent" to one another (see e.g., Fig. 1).

Regarding claim 7, Hikita et al. discloses in e.g., Fig. 1 said first (P13 and P14) and second (P11 and P12) terminal pairs being located at opposite ends of said first side of said integrated circuit package (1; see e.g., Fig. 1).

Regarding claim 21, Hikita et al. discloses in e.g., Fig. 1 an integrated circuit comprising:

- a semiconductor substrate (the substrate of the chip 2) having a first pair of bonding pads (P23 and P24) conducting a differential output signal thereon (column 4, lines 4 – 20) and adapted to be coupled to an input (222) of an external filter (22), and a second pair of bonding pads (P21 and P22) conducting a differential input signal thereon and adapted to be coupled to an output (221) of said external filter (22; see e.g., Fig. 1); and
- an integrated circuit package (1 and 40) encapsulating said semiconductor substrate (the substrate of the chip 2) and having at least first and second sides, and comprising a first pair of terminals (P13 and P14) located at a first end of said first side and coupled to said first pair of bonding pads (see e.g., Fig. 1), and a second pair of terminals (P11 and P12) located at a second end of said first side opposite said first

end and coupled to said second pair of bonding pads (see e.g., Fig. 1 and column 4, lines 21 – 32).

Furthermore, it has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. In re Hutchison, 69 USPQ 138.

Regarding claim 22, Hikita et al. discloses in e.g., Fig. 1 said integrated circuit package comprising four sides.

Regarding claim 23, Hikita et al. discloses in e.g., Fig. 1 said integrated circuit package further comprises a thin quad flat package (TQFP; since the package of Hikita et al. is a "thin", four sides and flat, the Hikita et al. fully meets this limitation.).

6. Claims 15 – 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Dreifus et al. (U. S. Pat. No. 5,576,589).

Regarding claim 15, Dreifus et al. discloses in e.g., Fig. 2 an integrated circuit comprising:

- a semiconductor substrate (21; column 6, line 38) having first, second, third, and fourth quadrants having respective first, second, third, and fourth bonding pads (26; see e.g., Fig. 2) located therein (see e.g., Fig. 2), said semiconductor substrate (21) including a first circuit (25, at the right-side) adapted to be coupled to a first external filter (24, at the right-side) coupled to said first circuit through said first and second bonding pads (26, at the right-side), and a second circuit (25, at the left-side) adapted

to be coupled to a second external filter (24, at the left-side) coupled to said second circuit through said third and fourth bonding pads (26, at the left-side); and

- an integrated circuit package (the external integrated circuits device that is attached to the element 21; column 6, lines 33 and 34) encapsulating said semiconductor substrate (21) and having first, second, third, and fourth terminals (the pads on the external integrated circuits device that are attached to the elements 26) corresponding and coupled to said first, second, third, and fourth bonding pads, respectively (see e.g., Fig. 2 and column 6, lines 33 and 34).

Furthermore, it has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. In re Hutchison, 69 USPQ 138.

Regarding claim 16, Dreifus et al. discloses in e.g., Fig. 2 said first and second circuits (25s in the both sides) comprising portions of radio frequency (RF) receivers (column 8, lines 20 – 22).

Regarding claim 17, the limitation "said first circuit comprises a portion of a satellite receiver and said second circuit comprises a portion of a terrestrial receiver" is an intended use language that does not structurally or patentably distinguish the claimed invention from the structure as disclosed by Dreifus et al. Furthermore, since any one of the first and second circuits are capable of performing as a satellite receiver or a terrestrial receiver, Dreifus et al. fully meets this limitation.

Regarding claim 18, Dreifus et al. discloses in e.g., Fig. 2 said first and second circuits (25s in the both sides) having "substantially" the same layout (see e.g., Fig. 2).

Regarding claim 19, Dreifus et al. discloses in e.g., Fig. 2 said first and second circuits (25s in the both sides) being adapted to be coupled to first and second external surface acoustic wave (SAW) filters (24; column 6, lines 36 – 46), respectively (see e.g., Fig. 2). Furthermore, it has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. In re Hutchison, 69 USPQ 138.

7. Claims 26, 27 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Hazama et al. (U. S. Pat. No. 4,296,391).

Regarding claim 26, Hazama et al. discloses in e.g., Fig. 9B an integrated circuit comprising:

- adjacent first (41; column 9, lines 67 – 68) and second (41') terminals at a first end of a first side of the integrated circuit (20; column 7, line 34) adapted to be coupled to a differential input (23 and 26; column 9, line 65) of a first external filter (the VHF filter; column 9, line 66);
- adjacent third (42; column 10, lines 1 and 2) and fourth (42') terminals at a second end of said first side of the integrated circuit (20) adapted to be coupled to a differential output (24 and 25; column 9, line 68) of said first external filter (the VHF filter; see e.g., Fig. 9B);
- adjacent fifth (43; column 10, line 5) and sixth (43') terminals at a first end of a second side of the integrated circuit (20) adapted to be coupled to a differential input

(29 and 32; column 10, line 2) of a second external filter (the UHF filter; column 10, line 3); and

- adjacent seventh (44; column 10, line 8) and eighth (44') terminals at a second end of said second side of the integrated circuit (20) adapted to be coupled to a differential output (30 and 31; column 10, lines 5 and 6) of said second external filter (the UHF filter; see e.g., Fig. 9B).

Regarding claim 27, Hazama et al. discloses in e.g., Fig. 9B the integrated circuit comprises a quad flat package (since the package of Hazama et al. has four sides and flat, the Hazama et al. fully meets this limitation.).

Regarding claim 29, Hazama et al. discloses in e.g., Fig. 9B each of said first and second external filters comprising a surface acoustic wave (SAW) filter (column 4, lines 60 – 63).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 4, 8 – 14, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita et al.

Regarding claims 4 and 11, while Hikita et al. discloses the use of the first (claim 4 and claim 11) and second (claim 11) pluralities of intervening terminals, Hikita et al. does not disclose the specific number of the first and second pluralities of intervening terminals. It would

have been obvious to one having ordinary skill in the art at the time of the invention was made to determine the first and second pluralities of intervening terminals being twelve terminals, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 8 and 25, while Hikita et al. discloses the use of the semiconductor substrate and the integrated circuit package, Hikita et al. does not disclose third and fourth pair of bonding pads in the semiconductor substrate and third and fourth terminal pairs in the integrated circuit package. It would have been obvious to one having ordinary skill in the art at the time when the invention was made to duplicate the first and second pair of bonding pads onto a portion of a bigger semiconductor substrate to have the third and fourth pairs of bonding pads, also duplicating the first and second terminal pairs to have third and fourth terminal pairs in the integrated circuit package, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Regarding claim 9, Hikita et al., as modified, discloses said first and second predetermined amounts (the amount of the gaps between the circuits in the filters) corresponding to differences between an attenuation in a stopbands of said first and second external filters, respectively.

Regarding claim 10, Hikita et al., as modified, discloses said first and second terminal pairs being located along a first side of said integrated circuit package (1) and separated by a first plurality of intervening terminals and said third and fourth terminal pairs being located along a

second side of said integrated circuit package and separated by a second plurality of intervening terminals.

Regarding claim 12, the limitation "said first and second pluralities of intervening terminals comprises at least one power supply terminal" is an intended use language that does not structurally or patentably distinguish the claimed invention from the structure as disclosed by Hikita et al. Furthermore, since any one of the first and second pluralities of intervening terminals is capable of performing as a power supply terminal, Hikita et al. fully meets this limitation.

Regarding claim 13, Hikita et al., as modified, discloses first and second terminals of each of said first, second, third, and fourth terminal pairs being adjacent to one another.

Regarding claim 14, Hikita et al., as modified, discloses said first and second terminal pairs being located at opposite ends of said first side of said integrated circuit package and said third and fourth terminal pairs being located at opposite ends of said second side of said integrated circuit package.

Regarding claim 24, while Hikita et al. discloses the use of the thin quad flat package (TQFP), Hikita et al. does not disclose the specific number of the terminals having 64-lead TQFP. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to determine the thin quad flat package (TQFP) having 64-leads, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980)

10. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dreifus et al. in view of Hayashi (U. S. Pat. No. 6,329,715).

While Dreifus et al. discloses the use of the first, second, third and fourth bonding pads, Dreifus et al. does not disclose fifth, sixth, seventh, and eighth bonding pads. Hayashi teaches in e.g., Fig. 1 a semiconductor substrate (1; column 7, lines 41 – 50) comprising fifth (301), sixth (302), seventh (303), and eighth (304) bonding pads respectively located in said first, second, third, and fourth quadrants (see e.g., Fig. 1) and forming complementary signal pairs with signals conducted on said first (32), second (311), third (312), and fourth (33) bonding pads, respectively (see e.g., Fig. 1 and column 7, lines 53 – 56). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the fifth, sixth, seventh, and eighth bonding pads of Hayashi onto the semiconductor substrate of Dreifus et al. as taught by Hayashi to provide ground pads for grounding (column 8, lines 47 and 48).

11. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hazama et al.

While Hazama et al. discloses the use of the terminals, Hazama et al. does not disclose the number of the terminal being sixty four and assignment of pin numbers to the terminals. It would have been obvious to one having ordinary skill in the art at the time when the invention was made to determine the terminals being sixty four and to assign pin numbers to the terminals, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art for the purpose of defining and identifying which operation each terminal would perform within the integrated circuit. Furthermore, see In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980) for the optimum value.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kawase et al., Nakamura et al. and Onishi et al. disclose a surface acoustic wave device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

KENNETH PARKER
SUPERVISORY PATENT EXAMINER

c.c.
Thursday, April 13, 2006